

# Electrical and structural properties of double metal structure Ni/V Schottky contacts on *n*-InP after rapid thermal process

S. Sankar Naik · V. Rajagopal Reddy ·  
Chel-Jong Choi · Jong-Seong Bae

Received: 29 June 2010/Accepted: 20 October 2010/Published online: 11 November 2010  
© Springer Science+Business Media, LLC 2010

**Abstract** The electrical, structural, and surface morphological properties of Ni/V Schottky contacts have been investigated as a function of annealing. The Schottky barrier height value from *I*–*V* and *C*–*V* measurements for as-deposited Ni/V/*n*-InP diode is 0.61 eV (*I*–*V*) and 0.91 eV (*C*–*V*), respectively. It has been observed that the Schottky barrier height decreases with increasing annealing temperature as compared to the as-deposited contact. For the contact annealed at 200 °C, the obtained barrier height decreased to 0.52 eV (*I*–*V*) and 0.78 eV (*C*–*V*). Further, the annealing temperature increased to 300 and 400 °C, the barrier height slightly increased to 0.58 eV (*I*–*V*), 0.82 eV (*C*–*V*) and 0.59 eV (*I*–*V*), 0.88 eV (*C*–*V*). However, after annealing at 500 °C, results then decrease in barrier height to 0.51 eV (*I*–*V*) and 0.76 eV (*C*–*V*), which is lower than the value obtained for the sample annealed at 200 °C. The Norde method is also employed to extract the barrier height of Ni/V/InP Schottky diode, and the values are 0.68 eV for the as-deposited and 0.56 eV for the contact annealed at 500 °C, which are in good agreement with those obtained by *I*–*V* technique. Based on the results of AES and XRD studies, it is concluded that the formation of indium phases at the Ni/V/*n*-InP interface may be the reason for the

increase in the barrier height for the as-deposited contact. The decrease in the barrier height upon annealing at 500 °C may be due to the formation of phosphide phases at the interface. The AFM results showed that there is no significant degradation in the surface morphology (RMS roughness of 0.61 nm) of the contact even after annealing at 500 °C.

## Introduction

A large effort has been made on the study of metal–InP interfaces in the last few years. This interest is to deal the growing technical application of the InP-based devices, as well as form a basic interest in the physical mechanisms responsible for Schottky barrier formation. Metal film deposition on InP substrates has received much attention for many years because of interest to develop fabrication technology for high-speed devices. Schottky barrier contacts based on *n*-InP are of considerable interest on account of their potential applications in gate electrode of a field-effect transistor (MESFET), microwave devices, high-speed charge-coupled devices, and solar cells [1–3]. Metal–semiconductor (MS) contacts are one of the most widely used rectifying contacts in electronic industry [4–6]. Schottky contacts play an important role in controlling the electrical performance of semiconductor device and Schottky barrier height (SBH). The SBH is highly sensitive to thermal treatment of the metal–semiconductor interfaces.

Normally, InP Schottky diode shows low barrier heights than desirable due to many reasons. One reason may be the out-diffusion of InP atoms into the adjoining metal films leaving vacancies or more complex defects within the band gap pinning the Fermi level [7]. Another possibility is that the chemical reactions and/or out-diffusion occurring at the

S. Sankar Naik · V. Rajagopal Reddy (✉)  
Department of Physics, Sri Venkateswara University,  
Tirupati 517502, India  
e-mail: reddy\_vrg@rediffmail.com

C.-J. Choi  
School of Semiconductor and Chemical Engineering,  
Semiconductor Physics Research Center (SPRC),  
Chonbuk National University, Jeonju 561-756, Korea

J.-S. Bae  
Busan Center, Korea Basic Science Institute (KBSI),  
Busan 609-735, Korea

metal–InP interface produce interfacial layers, which contribute to the barrier by local charge redistribution and/or effective work function change at the interface [8]. Moreover the realization of *n*-InP Schottky diodes is hindered by low barrier heights, unstable ohmic contacts with moderate resistivity, poor surface morphology, and large reverse current [9], even though Schottky barrier diodes with low barrier heights have found applications as infrared detectors in devices operating at cryogenic temperatures and as sensors in thermal imaging [10]. In order to make metal contacts with improved thermal and electrical stability as well as desirable morphologies, it is important to have a good understanding of the reactions of the contact metals with InP, as the performance and reliability of Schottky barrier diodes are drastically influenced by the quality of interface between the deposited metal and the semiconductor surface. Hence, formation and characterization of metal/InP devices have been the subject of vast number of fundamental studies. Formation of semiconductor devices involves annealing at various temperatures. Therefore, it is necessary to understand what happens to the metal contacts during the annealing process.

Various metals have used for the formation of Schottky contacts on *n*-InP by many research groups [11–20]. Cetin et al. [11] fabricated Au and Cu/*n*-InP Schottky barrier diodes and reported that the effective barrier height of the Au and Cu Schottky contacts are 0.480, 0.404 and 0.524 eV, 0.453 eV from *I*–*V* and *C*–*V* measurements. Miyazaki et al. [12] investigated the electrical properties of Ni/Al Schottky contacts on *n*-InP and reported that the barrier height was enhanced after thermal annealing. Chen and Chou [13] investigated the hydrogen sensing performance of Pd/*n*-InP Schottky diodes. They found that the changes in the Schottky barrier height and ideality factor are increased with the increase of hydrogen concentration. Haung et al. [14] prepared a high performance double metal structure using Pt and Al as Schottky contacts on *n*-InP and reported an effective barrier height of 0.74 eV. Cetin and Ayyildiz [15] fabricated Au, Al, and Cu/*n*-InP (100) Schottky barrier diodes on *n*-InP surfaces and investigated the influence of the air-grown oxide on the electrical performance. Janardhanam et al. [16] fabricated Mo Schottky diode on *n*-InP and investigated the electrical, structural, and surface morphological properties as a function of annealing temperature. They reported that the decrease in barrier height after annealing at 500 °C may be due to the formation of phosphide phases at the interface. Recently, Bhaskar Reddy et al. [17] investigated the effect of rapid thermal annealing on the electrical and structural properties of Ni/Au Schottky contacts to *n*-InP. They reported that the barrier height of as-deposited was high. They concluded that it may be due to the formation of indium interface products at the interface. In this study,

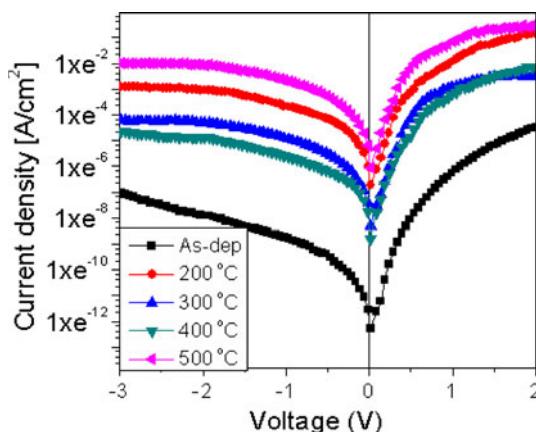
vanadium (V) is selected as the first Schottky layer because it has low work function as well as to provide the lowest forward voltage drop. The transition metal nickel (Ni) is used as the second Schottky metal layer because it has a high metal work function, high reliability, and high reactivity with InP. In this article, we investigate the electrical, structural, and surface morphological properties of Ni/V Schottky contacts on *n*-type InP as a function of annealing temperature.

## Experimental details

The samples used in this study are liquid encapsulated Czochralski grown undoped *n*-type InP (100) having a carrier concentration of  $4.9\text{--}5.0 \times 10^{15} \text{ cm}^{-3}$ . InP wafer is initially degreased with warm organic solvents like trichloroethylene, acetone, and methanol by means of ultrasonic agitation for 5 min each step, to remove contaminants followed by rinsing in deionized (DI) water and then dried in N<sub>2</sub> flow. The InP samples are then etched with HF (49%) and H<sub>2</sub>O (1:10) to remove the native oxides from the substrate. Ohmic contacts of thickness 500 Å are formed with indium on the rough side of the InP wafer prior to Schottky contact fabrication under the pressure of  $7 \times 10^{-6}$  mbar during deposition. The contacts are then annealed at 350 °C for 60 s in N<sub>2</sub> atmosphere. A metallization scheme of Ni/V thickness of 300 Å of each with a diameter of 0.7 mm is deposited on the polished side of the InP wafer through a stainless steel mask under a vacuum pressure of  $6 \times 10^{-6}$  mbar. The Schottky contacts are annealed in the temperature range 200–500 °C for duration of 1 min in N<sub>2</sub> flow using rapid thermal annealing (RTA) system. The current–voltage (*I*–*V*) and the capacitance–voltage (*C*–*V*) characteristics of Ni/V Schottky contacts have been measured using Keithly source measuring unit (Model No 2400) and DLS-83D spectrometer at room temperature. Auger electron spectroscopy (AES: UG: micro lab 350) depth profile has been performed to examine the intermixing of the metal and InP before and after annealing. X-ray diffraction (Siefert XRD PW 3710 using Cu K $\alpha$  radiation) has been carried out to characterize the interfacial reactions between the metal and InP layers. Atomic force microscopy (AFM) has also been carried out to characterize surface morphology of Ni/V Schottky contacts before and after annealing.

## Results and discussion

Figure 1 shows the current density–voltage (*J*–*V*) characteristics of the Ni/V Schottky contacts to *n*-InP which are annealed at temperature in the range 200–500 °C. It is



**Fig. 1** The reverse and forward  $J$ - $V$  characteristics of the Ni/V Schottky contact on  $n$ -type InP as a function of annealing temperature

observed that the electrical characteristics of Ni/V/ $n$ -InP Schottky diodes are uniform over different diodes. The Schottky barrier height ‘ $\Phi_b$ ’ and ideality factor ‘ $n$ ’ are estimated using the following expression based on the thermionic emission (TE) theory and is given by [21]

$$J = J_0 \left[ \exp \left( \frac{qV}{nkT} \right) \right] \quad (1)$$

$$J_0 = A^{**} T^2 \exp \left( \frac{-q\Phi_b}{kT} \right) \quad (2)$$

where  $J_0$  is the saturation current density,  $\Phi_b$  is the Schottky barrier height,  $q$  is the charge of electron,  $V$  is the applied voltage,  $k$  is the Boltzmann’s constant,  $n$  is the ideality factor,  $T$  is the temperature in Kelvin, and  $A^{**}$  is the effective Richardson’s constant. The theoretical value of  $A^{**}$  is  $9.4 \text{ A cm}^{-2} \text{ K}^{-2}$  based on the effective mass ( $m^* = 0.078 m_0$ ) of InP and is used here to deduce  $\Phi_b$  [3]. The value of ‘ $\Phi_b$ ’ can also be deduced directly from the  $J$ - $V$  curves if the effective Richardson’s constant  $A^{**}$  is known. The plot of  $\ln(J)$  versus  $V$  is a straight line with a slope of  $q/(nkT)$  and the intercept on  $y$ -axis yields  $J_0$ . The barrier height is calculated using Eq. 2. The measured leakage current densities at  $-1 \text{ V}$  are  $1.61 \times 10^{-4}$  and  $3.73 \times 10^{-3} \text{ A}$  for the as-deposited and  $400 \text{ }^\circ\text{C}$  annealed samples. However, the leakage current density is increased to  $7.13 \times 10^{-2} \text{ A}$  at  $-1 \text{ V}$  when the contact is annealed at temperature  $500 \text{ }^\circ\text{C}$ . Calculations showed that the SBH is  $0.61 \text{ eV}$  for the as-deposited contact which agrees with the reported value for the Ru/InP Schottky diode by Barnard et al. [9]. The estimated Schottky barrier height for the samples annealed at  $200$ ,  $300$ ,  $400$ , and  $500 \text{ }^\circ\text{C}$  are  $0.52$ ,  $0.58$ ,  $0.59$ , and  $0.51 \text{ eV}$ , respectively. Further, it is observed that the barrier height slightly decreased with increase of annealing temperature. The ideality factor ‘ $n$ ’ is calculated from the forward characteristics using the relation  $n = (q/kT)(dV/d(\ln J))$ . The ideality factor is

determined from a plot of natural log of current density versus forward bias voltage for small forward current where the effect of series resistance is small. The ideality factor of the as-deposited Ni/V/ $n$ -InP Schottky diode has been found to be  $1.6$ . The ideality factor is increased to  $2.3$  upon annealing at  $500 \text{ }^\circ\text{C}$  for  $1 \text{ min}$  in nitrogen ambient. The higher values of ideality factor are probably due to potential drop in the interface layer, presence of excess current and the recombination current through the interfacial states between the semiconductor/insulator layers.

If the current transport is controlled by the thermionic field emission (TFE) theory due to the local enhancement of electric field which can also yield a local reduction of the barrier height, the  $J$ - $V$  characteristic in the presence of tunneling can be described by the relation [22, 23]

$$J = J_0 \exp \left[ \frac{qV}{E_{00} \coth(E_{00}/kT)} \right] \quad (3)$$

$$J_0 = \frac{A^{**} T \sqrt{\pi E_{00} q (\Phi_b - V - \xi)}}{K \coth(E_{00}/kT)} \times \exp \left[ -\frac{q\xi}{kT} - \frac{q}{E_{00} \coth(E_{00}/kT)} (\Phi_b - \xi) \right], \quad (4)$$

$$E_{00} = \frac{qh}{4\pi} \sqrt{\frac{N_d}{\epsilon_s m^*}} \quad (5)$$

where  $J$  is the observed current density of Schottky diodes under forward bias condition,  $m^*$  is the effective mass of the semiconductor,  $N_d$  is the doping concentration,  $\epsilon_s$  is the permittivity of the semiconductor ( $\epsilon_s = 11\epsilon_0$ ),  $E_{00}$  is the tunneling parameter,  $V$  is the voltage,  $q$  is the electron charge, and  $\xi$  is equal to  $\frac{E_F - E_V}{q}$ .  $E_V$  is the valence band maximum and  $E_F$  is the position of the Fermi level. The Schottky barrier height and the tunneling parameter of the as-deposited sample are determined to be  $0.67 \text{ eV}$  and  $1.19 \text{ meV}$ , respectively, by using Eqs. 3–5. For the contacts are annealed at  $200$ ,  $300$ ,  $400$ , and  $500 \text{ }^\circ\text{C}$ , the Schottky barrier height ( $\Phi_b$ ) and the tunneling parameters ( $E_{00}$ ) are found to be  $0.57$ ,  $0.63$ ,  $0.64$ , and  $0.53 \text{ eV}$  and  $1.38$ ,  $1.34$ ,  $1.27$ , and  $1.40 \text{ meV}$ , respectively. The ideality factor of the Schottky contacts is determined using  $n = \frac{E_{00}}{kT} \coth(\frac{E_{00}}{kT})$ . The ideality factor is obtained as  $1.2$  and  $2.0$  for the as-deposited contact and annealed at  $500 \text{ }^\circ\text{C}$ , respectively. Under the physical point of view, the TFE mechanism involves the electrons which do not have sufficient thermal energy to overcome the barrier, as in the case of classic thermionic emission, but their thermal energy is sufficient to tunnel at an energy than the Fermi level, i.e., where the barrier is thinner. The results of the TE and TFE calculations are summarized in Table 1. The values of ideality factor  $n$  are fairly similar to those obtained by the TE conduction, indicating that our calculation is valid.

**Table 1** Summary of the electrical characteristics of Ni/V Schottky contact on *n*-type InP using the TE and TFE relations as a function of annealing temperature

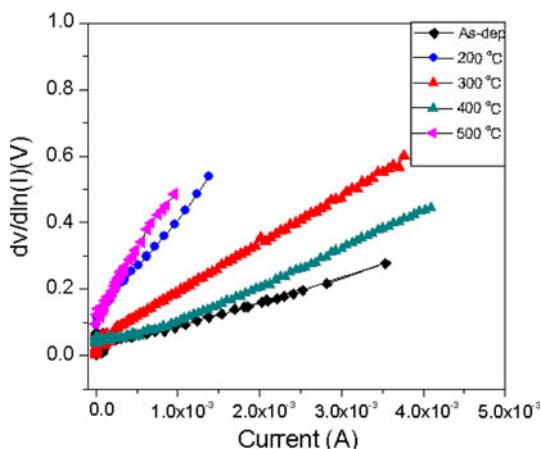
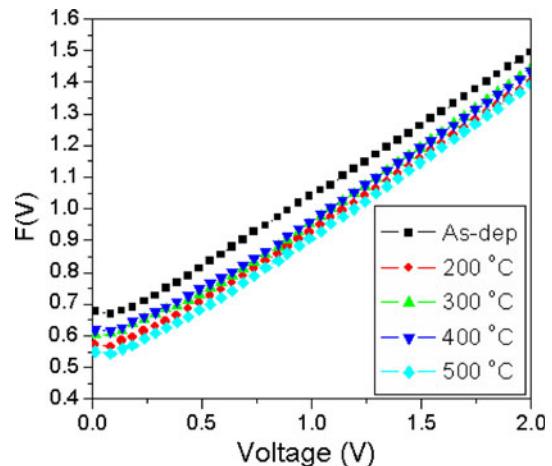
Sample ( °C)	Leakage current density at -1 V	TE conduction		TFE conduction			SBH (eV)		Series resistance $R_s$ (Ω)
		SBH (eV)	$n$	BH (eV)	$n$	$E_{00}$ (meV)	Norde	C-V	
As-dep	$1.62 \times 10^{-4}$	0.61	1.6	0.67	1.2	1.905	0.68	0.91	59
200	$2.59 \times 10^{-2}$	0.52	2.2	0.57	1.9	2.506	0.58	0.78	312
300	$7.59 \times 10^{-3}$	0.58	2.0	0.63	1.7	2.576	0.62	0.82	149
400	$3.73 \times 10^{-3}$	0.59	1.9	0.64	1.5	1.998	0.63	0.88	98
500	$7.14 \times 10^{-2}$	0.51	2.3	0.53	2.0	2.578	0.56	0.76	405

The series resistance  $R_s$  of the diode is calculated from  $I$ – $V$  measurement, using a method developed by Cheung and Cheung [24]. In this method the forward bias current–voltage characteristics due to thermionic emission of a Schottky contact with the series resistance can be expressed as Cheung's function given by,  $dV/d(\ln I) = IR_s + nkT/q$ . The plots experimental  $dV/d(\ln I)$  versus  $I$  for different temperatures are shown in Fig. 2. The estimated series resistance is in the range  $R_s = 59$ – $405 \Omega$  for the as-deposited and the contact annealed at  $500^\circ\text{C}$  Ni/V/*n*-InP Schottky diode. As high series resistance can hinder an accurate evolution of barrier height from the standard  $\ln(I)$ – $V$  plot, the Norde method [25] is also employed to compare the barrier heights of the Ni/V Schottky contacts. In this method, a function  $F(V)$  is plotted against  $V$ .  $F(V)$  is given by

$$F(V) = \frac{V}{2} - \frac{kT}{q} \ln\left(\frac{I(V)}{AA^{**}T^2}\right) \quad (6)$$

The effective Schottky barrier height is given by

$$\phi_b = F(V_{\min}) + \frac{V_{\min}}{2} - \frac{kT}{q} \quad (7)$$

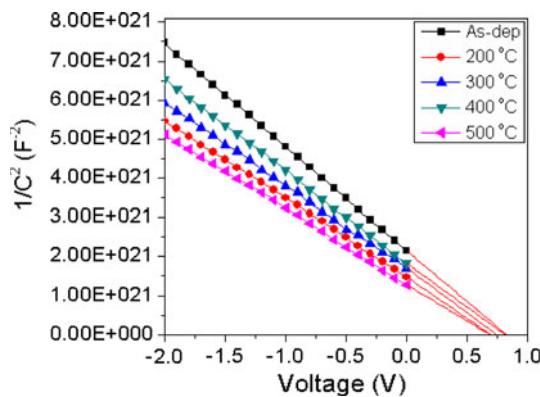
**Fig. 2** Plots of  $dV/d\ln(I)$  versus  $I$  for the Ni/V/*n*-InP Schottky diode as a function of annealing temperature**Fig. 3** Plot of  $F(V)$  against  $V$  for Ni/V Schottky contacts annealed at different temperatures

where  $F(V_{\min})$  is the minimum value of  $F(V)$ , and  $V_{\min}$  is the corresponding voltage. A plot of  $F(V)$  versus  $V$  for the sample annealed at different temperatures is shown in Fig. 3. The extracted Schottky barrier heights are 0.68 eV for the as-deposited, 0.58 eV at  $200^\circ\text{C}$ , 0.62 eV at  $300^\circ\text{C}$ , 0.63 eV at  $400^\circ\text{C}$ , and 0.56 eV at  $500^\circ\text{C}$ , respectively. It is noted that these values are in good agreement with those obtained by  $I$ – $V$  method.

Figure 4 shows the plot of  $1/C^2$  as a function of reverse bias voltage for the as-deposited and annealed Ni/V/*n*-InP Schottky diodes. The junction capacitance has been measured at a frequency of 1 MHz. The  $C$ – $V$  relationship for Schottky diode is given by [26]

$$\frac{1}{C^2} = \left( \frac{2}{\epsilon_s q N_d A^2} \right) \left( V_{bi} - \frac{kT}{q} - V \right) \quad (8)$$

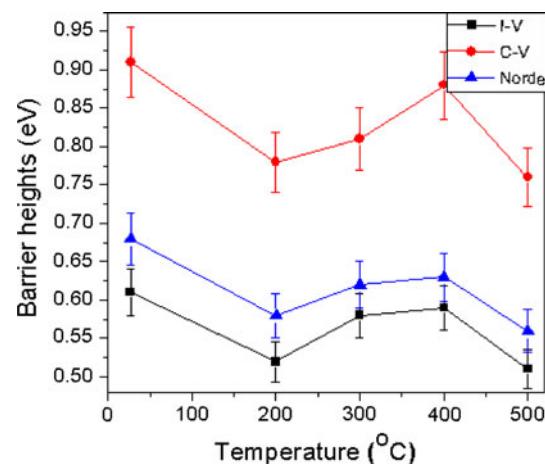
where  $\epsilon_s$  is the permittivity of the semiconductor ( $\epsilon_s = 11\epsilon_0$ ),  $V$  is the applied voltage,  $A$  is the surface area of the diode,  $N_d$  is the donor concentration, and  $V_{bi}$  is the flat band voltage. The  $x$ -intercept of the plot of  $(1/C^2)$  versus  $V$  gives  $V_0$ , where  $V_0$  is related to the built-in potential  $V_{bi}$  by the equation  $V_{bi} = V_0 + \frac{kT}{q}$ , where  $T$  is the absolute temperature. The



**Fig. 4** Plot of  $1/C^2$  against  $V$  for the Ni/V/n-InP Schottky contacts annealed at different temperatures

barrier height is given by the equation  $\phi_{CV} = V_{bi} + V_n$ , where  $V_n = \left(\frac{kT}{q}\right) \ln\left(\frac{N_c}{N_d}\right)$ . The density of states in the conduction band edge is given by  $N_c = 2(2\pi m^* \frac{kT}{h^2})^{3/2}$ , where  $m^* = 0.078 m_0$ , and its value is  $5.7 \times 10^{17} \text{ cm}^{-3}$  for InP [27]. The calculated carrier concentration of Ni/V Schottky contacts are  $3.27 \times 10^{15} \text{ cm}^{-3}$  for the as-deposited and  $4.37 \times 10^{15}$ ,  $4.09 \times 10^{15}$ ,  $3.71 \times 10^{15}$ , and  $4.51 \times 10^{15} \text{ cm}^{-3}$  for the contacts annealed at 200, 300, 400, and 500 °C, respectively, as determined from the slope of the curves. The measured Schottky barrier heights of Ni/V Schottky contact from these plot are 0.91 eV for as-deposited, 0.78, 0.82, 0.88, and 0.76 eV for samples annealed at 200, 300, 400, and 500 °C, respectively. Table 1 shows the value of leakage current densities, series resistance, Schottky barrier heights, and ideality factors at different annealing temperatures.

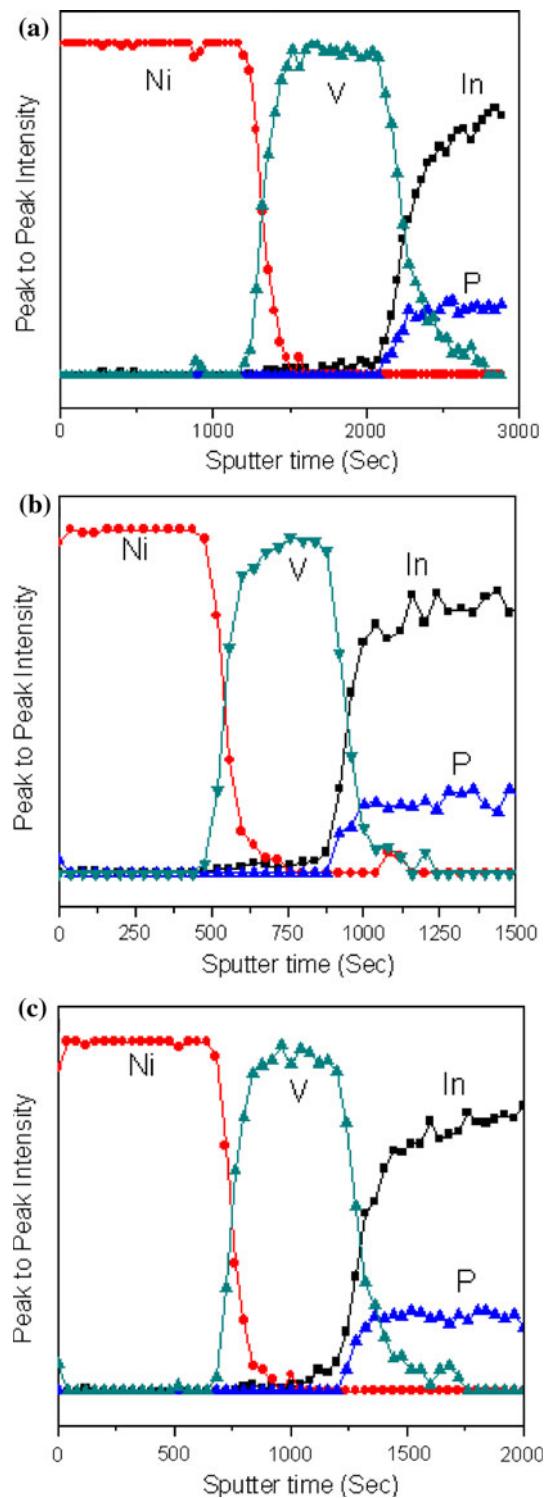
In order to compare the barrier heights which are obtained from different methods ( $I-V$ , Norde,  $C-V$ ), a plot drawn between the barrier heights and annealing temperature is shown in Fig. 5. It is observed that the barrier height of the Ni/V Schottky contact decreases upon annealing from 0.61 eV for the as-deposited to 0.52 eV for the contact annealed at 200 °C, respectively. However, the barrier height slightly increases to 0.59 eV when the contact is annealed at 400 °C. Further, increase in annealing temperature up to 500 °C, the Schottky barrier height (SBH) decreases to 0.51 eV as compared to the as-deposited and annealed contacts. It is evident from Fig. 5 that the barrier heights obtained from  $I-V$  measurements ( $\Phi_{IV}$ ) are lower than those obtained from  $C-V$  measurements ( $\Phi_{CV}$ ). The existence of barrier height inhomogeneity at the interface may play an important role in the difference between barrier heights measured by  $I-V$  and  $C-V$  methods. Since the interfacial capacitance and capacitance due to depletion layer are in series, the total capacitance decreases and as a result  $C^{-2}$  increases. This increases the



**Fig. 5** Plot of barrier heights against annealing temperatures for the Ni/V Schottky contacts on *n*-type InP

intercept of  $C^{-2}$  versus  $V$  plot which causes the barrier height high. Since the  $I-V$  method involves the flow of electrons from semiconductor to metal, the barrier height determined from this method will yield lower barrier heights. This is known as parallel [28] (or) mixed-phase [8] contact. Another possibility is the difference in the barrier height values obtained from the  $I-V$  and  $C-V$  measurements that may be due to the presence of an insulating layer (or) charges existing at the metal–semiconductor interface, the impurity levels, image force barrier lowering, and edge leakage currents [1, 21, 29].

The AES depth profiles of the Ni/V Schottky contacts on InP are shown in Fig. 6. Peak-to-peak intensities are recorded as a function of sputtering time and the results will be discussed only in the qualitative way. Comparison of the depth profile before and after annealing temperature, obtained in the same conditions, show that the main effect of thermal treatment is a strong diffusion at the metal–semiconductor interface. The as-deposited layer (Ni and V), Fig. 6a, exhibits a relative sharp interface, indicating the absence of significant interdiffusion into InP. It is noted that some amount of indium (In) is out-diffused into the metal layers. This is indicative of possible reactions between Ni/V layers and In, which would lead to the formation of the Ni– and V–In interfacial phases at the interface. However, for the sample annealed at 400 °C (Fig. 6b), a small amount of indium (In) is out-diffused into the metal layers, indicating possibility that In reacts with V to form V–In intermetallic compound during annealing temperature. Further, it is noted that some amount of phosphide is also out-diffused into the metal layers, indicating the formation of phosphate phases at the metal/semiconductor. However, it is observed that for the contact annealed at 500 °C, a large amount of In is out-diffused into the metal layers. The profile illustrates that a



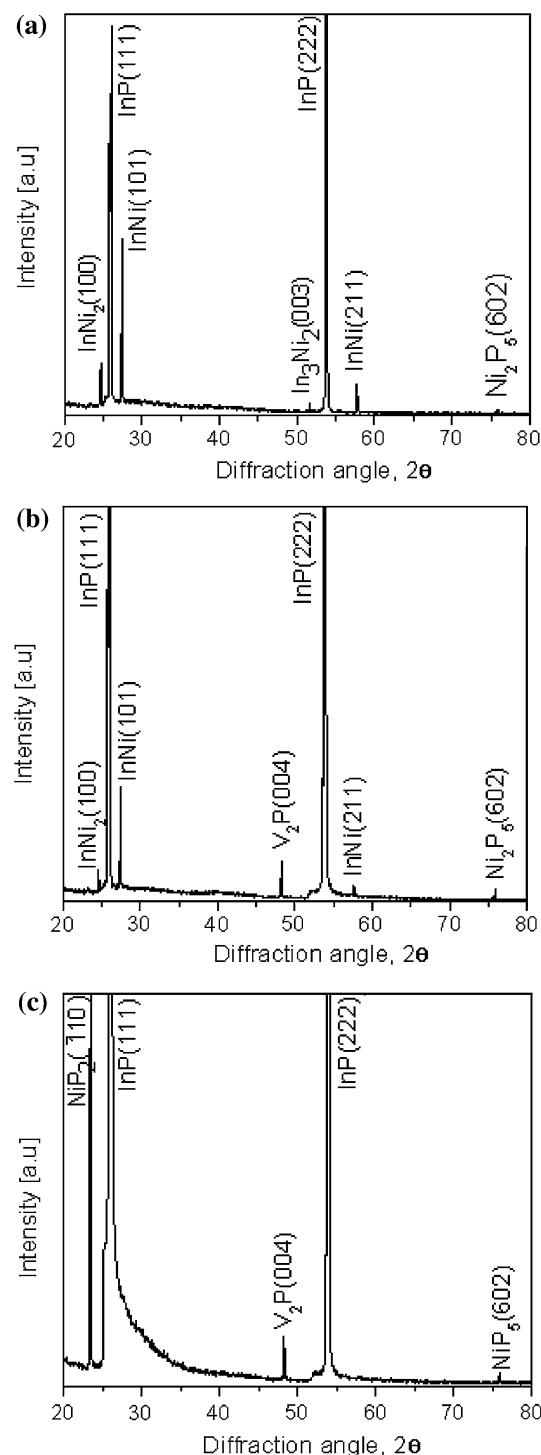
**Fig. 6** AES depth profile analysis of the Ni/V Schottky contacts on *n*-type InP: **a** as-deposited, **b** annealed at 400 °C, and **c** annealed at 500 °C

small amount of phosphate (P) is also out-diffused in the metal layer, which indicates the formation of N– and V–P interfacial phases at the interface as shown in Fig. 6c.

In order to investigate the interfacial reactions between metal and InP, XRD studies were carried out before and after annealing at 500 °C. Figure 7a shows the XRD plot of the as-deposited contact. In addition to the characteristic peaks of InP (111) (222), extra peaks are observed. These peaks are identified as InNi<sub>2</sub> (100), InNi (101), In<sub>3</sub>Ni<sub>2</sub> (003), InNi (211), and Ni<sub>2</sub>P<sub>5</sub> (602). Figure 7b shows the XRD plot of contact annealed at 400 °C. As can be seen from the plot, in addition to the peaks which are observed in the as-deposited contact, there is an additional peak, indicating the formation of new interfacial phases, which is identified as V<sub>2</sub>P (004). When the contact is annealed at 500 °C, Fig. 7c, there is an extra peak, which is identified as NiP<sub>2</sub> (110) in addition to the peaks observed in the as-deposited and 400 °C annealed contacts. The peaks corresponding to In<sub>3</sub>Ni<sub>2</sub> (003), InNi<sub>2</sub> (100), and InNi (101), (211) had disappeared in the 500 °C annealed contact, which were observed in the as-deposited and 400 °C annealed contacts.

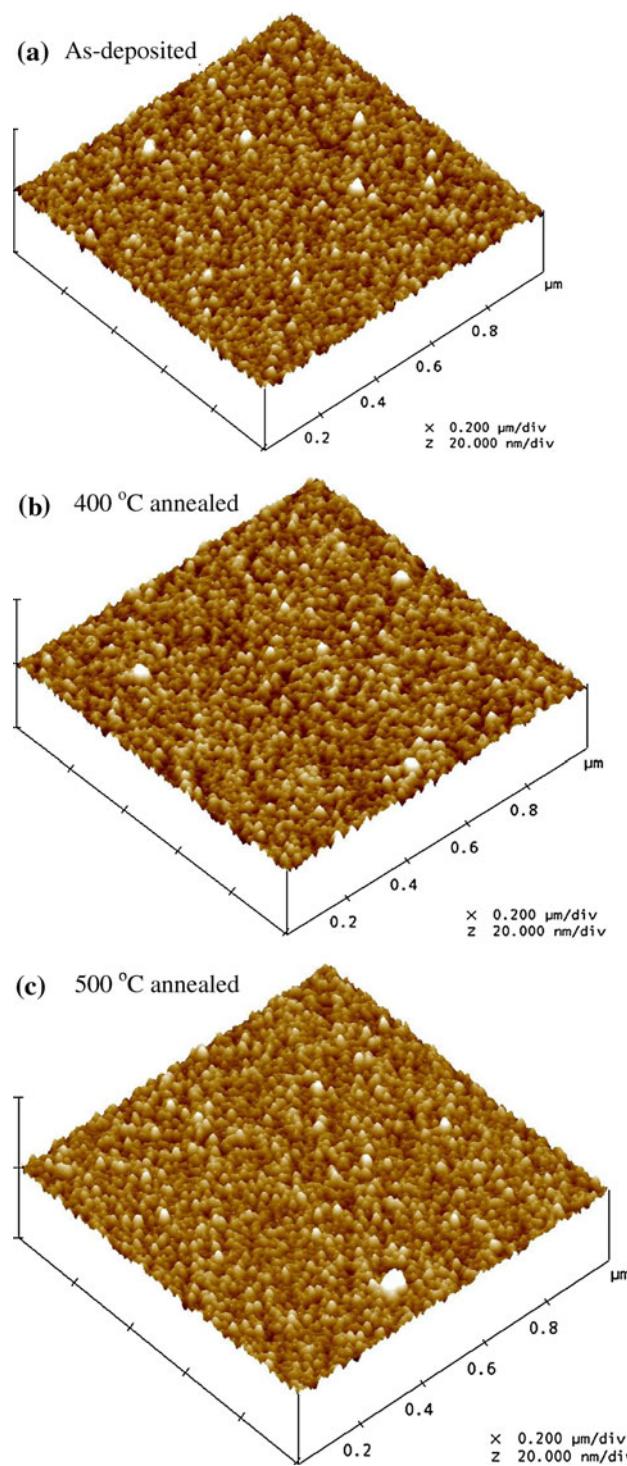
To characterize the surface morphology of the contacts, atomic force microscopy (AFM) measurement is performed. Figure 8 shows the AFM images of the contacts before and after annealing at 500 °C for 1 min in N<sub>2</sub> atmosphere. The surface morphology of as-deposited Ni/V contact is fairly smooth with a root mean square (RMS) roughness of 0.71 nm, as shown in Fig. 8a. When the contact is annealed at 400 °C, Fig. 8b, the surface morphology of the Ni/V Schottky contact is slightly improved with RMS roughness of 0.69 nm. However, for the contact annealed at 500 °C, the surface morphology became even smoother with an RMS roughness of 0.61 nm (Fig. 8c) as compared to the as-deposited and annealed at 400 °C samples. These results indicate that the Ni/V Schottky contact does not suffer from the thermal degradation during annealing temperature.

The interface states and chemical reactions between the metals and semiconductor interfaces play an important role in determining the electrical behavior of devices. The change in barrier height of the Ni/V Schottky contact with annealing temperature could be explained based on AES and XRD results. The AES and XRD results showed that for the Ni/V Schottky contacts, the diffusion of Ni and V and its reaction with InP form interfacial phases at the interfaces. Depending on these interfacial compounds the barrier heights may increase or decrease with increase in annealing temperature. The as-deposited Schottky contact shows the higher barrier height as compared to the annealed contacts. This may be due to the out-diffusion of In resulting in the formation of interfacial phases such as InNi<sub>2</sub> (100) and In<sub>3</sub>Ni<sub>2</sub> (003) at the interface as evidenced from XRD results. The increase in barrier height may be due to increase in negative charges at the interface that



**Fig. 7** The XRD plot of the Ni/V Schottky contacts on *n*-type InP: **a** as-deposited, **b** annealed at 400 °C, and **c** annealed at 500 °C

probably arises due to electron traps localized at the InP surface and associated with In vacancies created near the surface [30]. However, the increase of Schottky barrier height may also be due to the reduction of nonstoichiometric defects in metallurgical interface [7]. The reason



**Fig. 8** AFM micrographs of the Ni/V Schottky contacts on *n*-type InP: **a** as-deposited, **b** annealed at 400 °C, and **c** annealed at 500 °C

involving the defects can be reduced due to the interdiffusion of metals into InP. The decrease of barrier height upon annealing at 500 °C could be attributed to the reaction of Ni and V with the phosphorous resulting in the formation of  $\text{NiP}_2$  ( $\bar{1}10$ ) and  $\text{V}_2\text{P}$  (004) phases at the

interface. These interfacial phases may have different work functions than Ni and V contact layers, which is responsible for the variation of the barrier heights [21]. The presence of these phases at the interface causes the variation in leakage current. The formation of phosphorous phases may create phosphorous vacancies in InP layer near the junction and the phosphorus vacancies in InP act as donors, which reduce the barrier height after annealing as well as increase the ideality factor [31]. Similar findings are also observed by Reddy et al. [32] in GaN-related material. They observed that the barrier height would be influenced by interfacial products. Duboz et al. [33] also found that the Fermi level at metal/GaN interfaces is pinned by defects and a modification of the defect density on annealing could change the pinning, resulting in change in the barrier height. Van de Walle et al. [34] have also explained the barrier height change for annealed metal/*n*-GaAs Schottky barrier diodes by the relation between the equilibrium interface charge and barrier heights.

## Conclusions

Rapid thermal annealing effects on the electrical and structural properties of Ni/V Schottky contacts on *n*-type InP have been investigated using *I*–*V*, *C*–*V*, AES, and XRD measurements. The barrier height of the as-deposited Schottky diode is found to be 0.61 eV (*I*–*V*) and 0.91 eV (*C*–*V*). It is observed that the extracted barrier height of the as-deposited of Ni/V Schottky contact is high as compared to the annealed contacts. However, the barrier height is decreased to 0.52 eV (*I*–*V*) and 0.78 eV (*C*–*V*) after annealing at 200 °C for 1 min in N<sub>2</sub> ambient. Further, the barrier height is slightly increased to 0.58, 0.59 eV (*I*–*V*), and 0.82, 0.88 eV (*C*–*V*) when contacts are annealed at 300 and 400 °C, respectively. Moreover, with an increase in annealing temperature up to 500 °C, the SBH decreased to 0.51 eV (*I*–*V*) and 0.76 eV (*C*–*V*). The estimated the series resistance ( $R_s$ ) of Ni/V/*n*-InP Schottky diode is in the range 59–405 Ω for the as-deposited and annealed at 500 °C contacts. The AES and XRD results showed that InNi<sub>2</sub> (100) and In<sub>3</sub>Ni<sub>2</sub> (003) interfacial phases are formed at the metal/InP. This may be the reason for increase in the barrier height for as-deposited contact. The formation of phosphide phases at the interface after annealing at 500 °C may be the reason for decrease in the barrier height of Ni/V Schottky contacts as evidenced from the AES and XRD results. The atomic force microscopy (AFM) results showed that there is no significant degradation in the surface morphology (RMS roughness of 0.61 nm) of the Ni/V Schottky contact during annealed at 500 °C as compared

with that of the as-deposited sample (RMS roughness of 0.71 nm).

**Acknowledgments** This work was supported by the IT R&D program of MKE (KI002083, Next-Generation Substrate Technology for High Performance Semiconductor Devices).

## References

1. Tung RT (2001) Mater Sci Eng R 35:1
2. Lile DL, Collins DA (1980) Appl Phys Lett 37:552
3. Williams RH, Robinson GY (1985) Physics and chemistry of III–V compound semiconductor interfaces. Plenum Press, New York
4. Van Mairhaeghe RL, Lafleuri WH, Cardon F (1994) J Appl Phys 76:403
5. Arehart AR, Moran B, Speck JS, Mishra UK, DenBaars SP, Ringel SA (2006) J Appl Phys 100:023709
6. Marikita S, Ikoma H (2003) J Vac Sci Technol A 21:226
7. Spicer WE, Lindau I, Skeath P, Su CY, Chye P (1980) Phys Rev Lett 44:420
8. Freeouf JL, Woodall JM (1981) Appl Phys Lett 39:727
9. Barnard WO, Myburg G, Auret FD (1995) Vacuum 46:893
10. Chand S, Kumar J (1996) Appl Phys A 63:171
11. Cetin H, Ayyildiz E (2010) Physica B 405:559
12. Miyazaki S, Lin TC, Nishida C, Kaibe HT, Okumura T (1996) J Electron Mater 25:577
13. Chen H-I, Chou Y-I (2003) Semicond Sci Technol 18:104
14. Huang W-C, Dong-Rong Cai (2006) International workshop on junction technology, p 295
15. Cetin H, Ayyildiz E (2007) Physica B 394:93
16. Janardhanam V, Ashok Kumar A, Rajagopal Reddy V, Narasimha Reddy P (2009) Surf Interface Anal 41:905
17. Bhaskar Reddy M, Janardhanam V, Ashok Kumar A, Rajagopal Reddy V, Narasimha Reddy P (2010) Curr Appl Phys 10:687
18. Monch W (2008) Appl Phys Lett 93:172118
19. Eftekhari G (1995) Semicond Sci Technol 10:1163
20. Bhaskar Reddy M, Janardhanam V, Ashok Kumar A, Rajagopal Reddy V, Narasimha Reddy P (2009) Phys Status Solidi A 206:250
21. Rhoderick EH, Williams RH (1988) Metal-semiconductor contacts, 2nd edn. Clarendon Press, Oxford
22. Shur Michael (1990) Physics of semiconductor devices. Prentice-Hall, Engel-wood, Cliffs, NJ
23. Morkoc H (1999) Nitride semiconductors and devices. Springer, Berlin
24. Cheung SK, Cheung NW (1986) Appl Phys Lett 49:85
25. Norde H (1979) J Appl Phys 50:5052
26. Eftekhari G (1993) J Vac Sci Technol B 11:1317
27. Sze SM (1981) Physics of semiconductor devices. John Wiley & Sons, New York
28. Freeouf JL, Jackson TN, Laux SE, Woodall JM (1982) Appl Phys Lett 40:634
29. Crowel CR (1977) Solid State Electron 20:175
30. Cetin H, Ayyildiz E, Turut A (2005) J Vac Sci Technol B 23:2436
31. Haung TS, Fang RS (1994) Solid State Electron 37:1461
32. Rajagopal Reddy V, Koteswara Rao P (2008) Microelectron Eng 85:470
33. Duboz JY, Binet F, Laurent N, Rosencher E, Scholz F, Harle V, Briot O, Gil B, Aulombard RL (1996) Mater Res Soc Symp Proc 449:1085
34. Van de Walle R, Van Meirhaeghe RL, Lafleuri WH, Cardon F (1993) J Appl Phys 74(3):1885